Job Offer Reference:

Senior IC Layout Designer – SILD – September 22nd, 2015

Description

The IC layout Designer will work in the R&D team and will contribute to the development of innovative IP for secure products with embedded Flash.

The candidate as part of the layout team, will work on analog and mixed signals full custom layouts generation on the block and full chip level in advanced CMOS technologies.

He must be able to handle all aspects of layout such as signal integrity, parasitic constraints, IP placement constraints and layout verifications.

The candidate must be able to work in a stressful, challenging and team environment while following the layout flow and guidelines.

Qualifications

Minimum of 5+ years' experience in IC layout/mask design.

Skills

The applicant skills should include:

- Proficient with Cadence Virtuoso tool suite.
- Experience with physical verification tools, such as Calibre. (LVS, DRC).
- Experience in the area of Analog and NVM Flash design.
- Experience in full chip activity like floor plan, power routing plan and top-level layout verification.
- Experience in IO/ESD constraints.
- Experience in RFID and secure IP are a plus.

Applying

Please send your cover letter and resume to job@invia.fr